REMARKS

In this application, Claims 1, 20 and 26 have been amended. No claim is canceled and no claim is added.

Applicants respectfully requests reconsideration in light of the following remarks.

CLAIM REJECTIONS- 35 U.S.C. SECTION 102

Claims 1 and 3-5 stand rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al.(USPN 6,465,308).

Cheng et al. provides a structure and a process for manufacturing semiconductor devices with improved ESD protection for high voltage applications. A thick field gate oxide N channel FET device with a tunable threshold voltage (Vt) developed at the input/output to the internal active circuits for the purpose of providing ESD protection for applications in the 9 volt and higher range is provided. The device has a N-field dopant region under the thick oxide gate element which has the effect of modifying the threshold voltage (Vt) of this device enabling the device turn-on to be "tuned" to more closely match the application requirements of the internal semiconductor circuits, a gate and adrain of the thick oxide FET device connected to the input/output connection pad of the internal semiconductor circuits which also enhances ESD protection, and a FET source element is connected to another voltage source, typically ground. The device provides a path to shunt the current from an ESD incident thereby protecting the internal circuitry from damage.

The Examiner is of the opinion that the figure 7 of Cheng et al. shows all elements recited in claim 1, for example, a p type semiconductor bulk substrate 22, a first doped region of n^+ type 26, a second doped region of n^+ type 28, a channel 30 extends between 26 and 28, "the first gate segment" 38, and "first field oxide stripe" 24. And the Examiner thinks that "the first gate segment" 38 and "first field oxide stripe" 24 disclosed in Cheng et al. match the limitations about the first gate segment and the first field oxide stripe recited in Claim 1, even both of "the first gate segment" 38 and "first field oxide stripe" 24 disclosed in Cheng et al. are formed over all parts of the channel. It is because that Claim 1 does not say "the first gate segment is only formed over the first part of the channel" and "the first field oxide stripe is only formed over the second part of the channel".

In the present invention (see claim 1, 3-4 and 9-11, Fig. 5A, and Fig. 6A), the channel is formed between the first doped region and the second doped region, and it has a first part, a second part and a third part. The first part and the third part of the channel are the two ends of the channel respectively and the second part is located between the first part and the third part of the channel. In the present invention, the first gate segment is only formed the first part of the channel, and the first field-oxide stripe is only formed over the second part of said channel region.

However, according to the figure 7 and the specification of Cheng et al., we know that "the first field oxide stripe" 24 covers all parts of the channel 30, and all parts of "the first gate segment" 38 overlaps "the first field oxide stripe" 24 and covers all parts of the channel 30. The position and the relationship of "the first field oxide stripe" 24 and "the first gate segment" 38 are different from that of the first gate segment and the first field oxide stripe of the present invention. In the present invention, the first gate segment and the first field oxide stripe do not need to cover all parts of the channel (the first part, the second part and the third part). The first gate segment only covers the first part of the channel and the first field oxide stripe only

covers the second part of the channel. Besides, in the present invention, only one end of the first gate segment overlaps the first field oxide stripe, but in Cheng et al., all parts of "the first gate segment" 38 overlaps "the first field oxide stripe" 24. Thus, the structure of ESD protection device of the present invention is different from the structure of ESD protection device of Cheng et al., and the present invention isn't disclosed by the Cheng et al.. In the application, Claim 1 have been amended to depicted the above-mentioned feature to show what is the difference between the present invention and Cheng et al.. Therefore, according to above interpretation and amendment, the rejection of the claim 1 and 3-5 can be traversed.

CLAIM REJECTIONS- 35 U.S.C. SECTION 103

Claims 6-9, 11-13 and 26 stand rejected under 35 U.S.C. 103(a) as being anticipated over Cheng et al. in view of Lin et al., 6,574,568.

The Examiner is of the opinion that Lin et al. has disclosed or taught the type of islands, the position of the islands, the second gate segment, the position of the second gate segment, and etc..

Lin et al. provides ESD protection devices with a lower trigger voltage and the method forming the same by employing the thin gate oxide fabricated by a dual gate oxide process. The ESD protection device has a NMOS having islands with thin gate oxides and a control gate with a thick gate oxide. These islands overlap the drain region of the NMOS to reduce the breakdown voltage of the PN junction in the drain region, thereby reducing the ESD trigger voltage and improving the ESD protection level of the NMOS.

To view figure 3-5 and the specification of the Lin et al. (see column 5, lines 40-44), the two type of islands (20a and 20b) are disclosed by Lin et al. are

polysilicon-over-oxide, and the only difference between the island 20a and the island 20b is the thickness of the gate oxide. However, In the present invention, there are two type of islands which are formed over the bulk and encircled by the first doped region; one type of islands have polysilicon-over-oxide and another type of islands have field-oxide. Thus, the Lin et al. only discloses the type of the islands having polysilicon-over-oxide, but don't mention and teach another type of islands having field-oxide. Thus, according to above interpretation and amendment, the rejection of the claim 6-8 and 26 can be traversed.

According to above interpretation and amendment for "CLAIM REJECTIONS-35 U.S.C. SECTION 102", the structure of ESD protection device of the present invention is different from the structure of ESD protection device of Cheng et al. It is because that the first field oxide stripe is only formed over the second part of the channel and the first gate segment is only formed over the first part of the channel. However in Cheng et al, "the first field oxide stripe" 24 and "the first gate segment" 38 covers all parts of the channel 30, and all parts of "the first gate segment" 38 overlaps "the first field oxide stripe" 24. Therefore, what recited in claim 1 is not disclosed by Cheng et al and the structure of ESD protection device of the present invention can not be disclosed or taught even the Cheng et al. is combined with the Lin et al. According to above interpretation and dependancy of claim 1, the rejection of the claim 6-9 and11-13 can be traversed. The above mentioned features about the channel, the first gate segment and the first field oxide stripe are added in Claim 26, and thus, the rejection of the Claim 26 can be traversed.

Conclusion

In the light of the above amendments and remarks, Applicant respectfully submits that all pending Claims 1, 3-9, 11-20, and 22-26 as currently amended are in condition for allowance. Accordingly, reconsideration is respectfully requested.

Respectfully submitted,

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